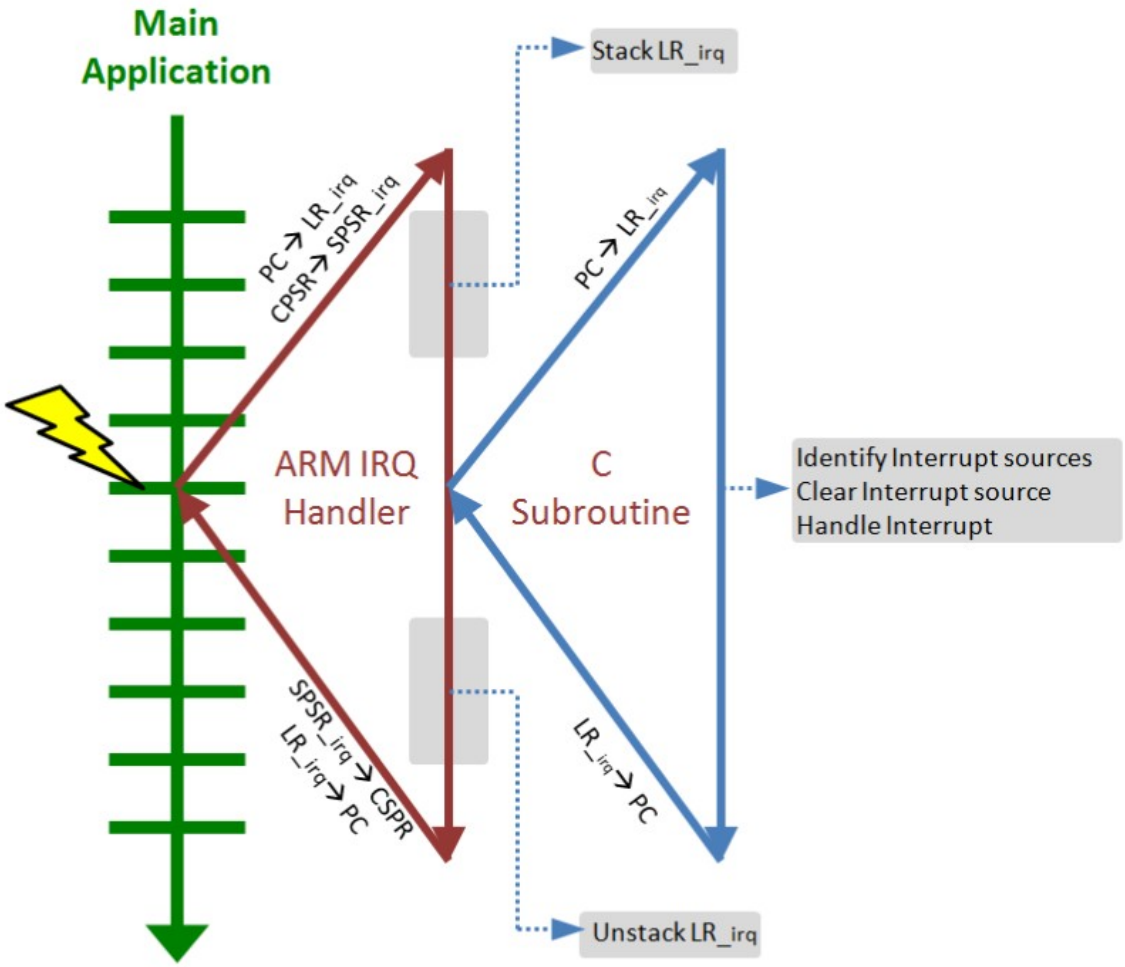

Interrupt Servicing in Cortex-A9

When an interrupt is received, the current executing instruction completes

* Save processor status
    - Copies CPSR into SPSR_irq
    - Stores the return address in LR_irq

* Change processor status for exception
    - Mode field bits ARM or thumb (T2) state
    - Interrupt disable bits (if appropriate)
    - Sets PC to vector address (either FIQ or IRQ)

(The above steps are performed automatically by the core)

* Executes top-level exception handler
    - The top-level handler branches to the appropriate device handler

* Return to main application
    - Restore CPSR from SPSR_irq
    - Restore PC from LR_irq
    - When re-enabling interrupts change to system mode (CPS)

(Above steps are the responsibility of the software)