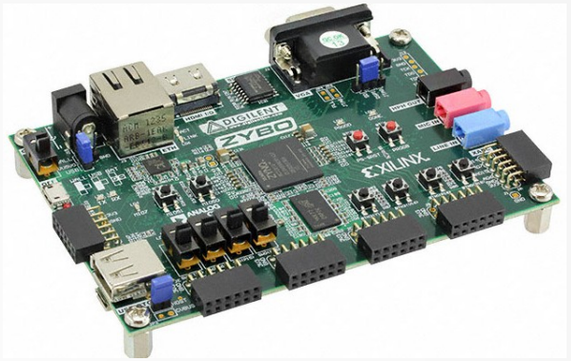
INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES TOULOUSE

LAAS



Course 01: Zynq architecture overview

CHERIF Bilel

5A-SIEC

Course material :

- A Practical Introductionto Hardware/Software Codesign.
- The zynq book.
- Xilinix Zynq TRM.
- AMBA Specification.
- The chronicles of microzed.
- Altera ARM A9 soc doccuments.

Course goals:

- Codesign: why ? And how ?
- Understand the main blocs functions in our architecture.
- Codesign process flow proposed by xilinix tools.

What is Software/Hardware Codesign ?

What is Software/Hardware Codesign ?

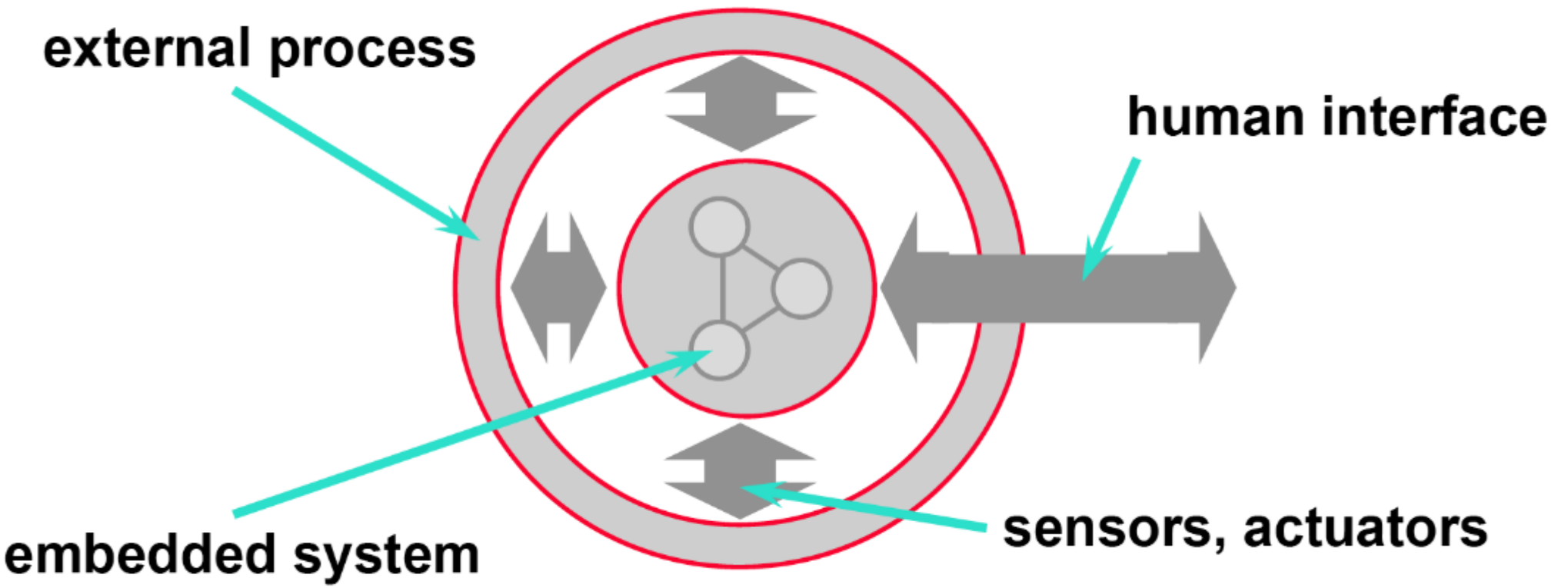
Hardware/software codesign investigates the concurrent design of hardware and software components of complex electronic systems. It tries to exploit the synergy of hardware and software with the goal to optimize and/or satisfy design constraints such as cost, performance, and power consumption of the final product. At the same time, it targets to reduce the time-to-market frame considerably.

Embedded Systems vs. General-Purpose Computing

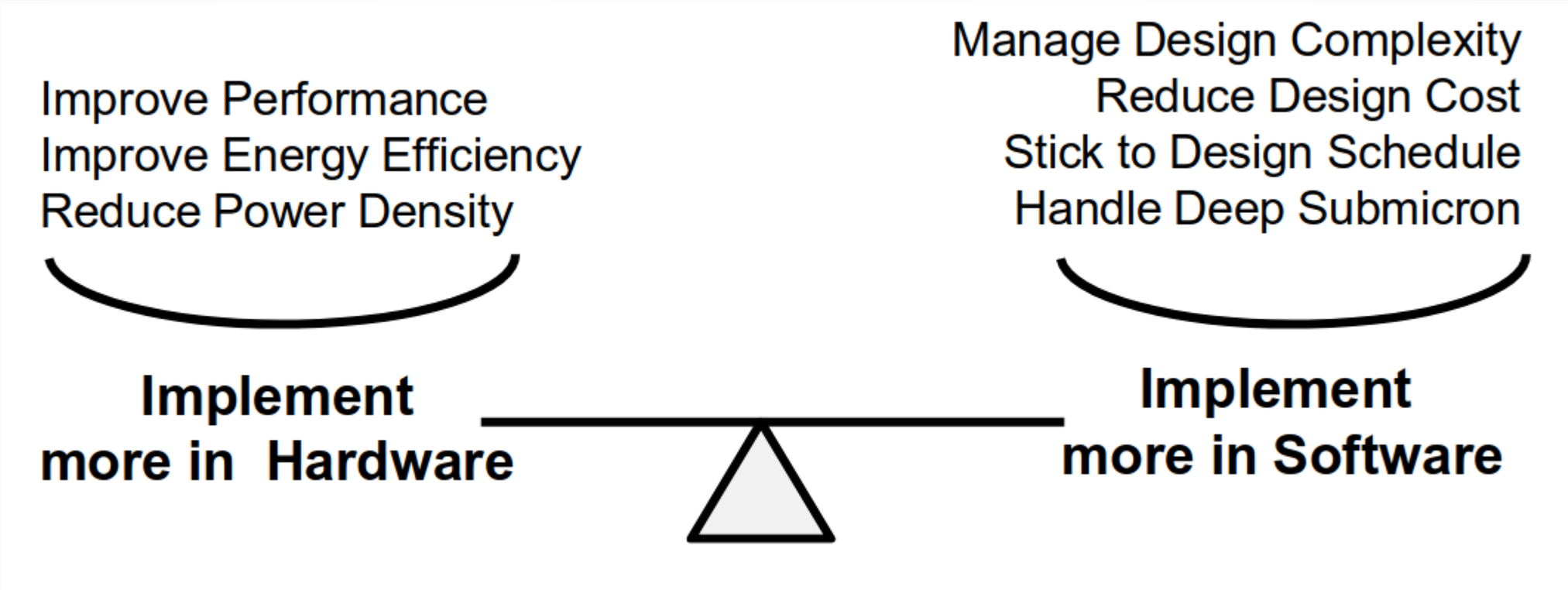
- **Embedded Systems**
  - Few applications that are known at design-time.
  - Not programmable by end user.
  - Fixed run-time requirements (additional computing power not useful).
  - Criteria:
    - cost
    - power consumption
    - predictability
    - meeting time bounds

- **General Purpose Computing**
  - Broad class of applications.
  - Programmable by end user.
  - Faster is better.
  - Criteria:
    - cost
    - average speed

Embedded Systems vs. General-Purpose Computing



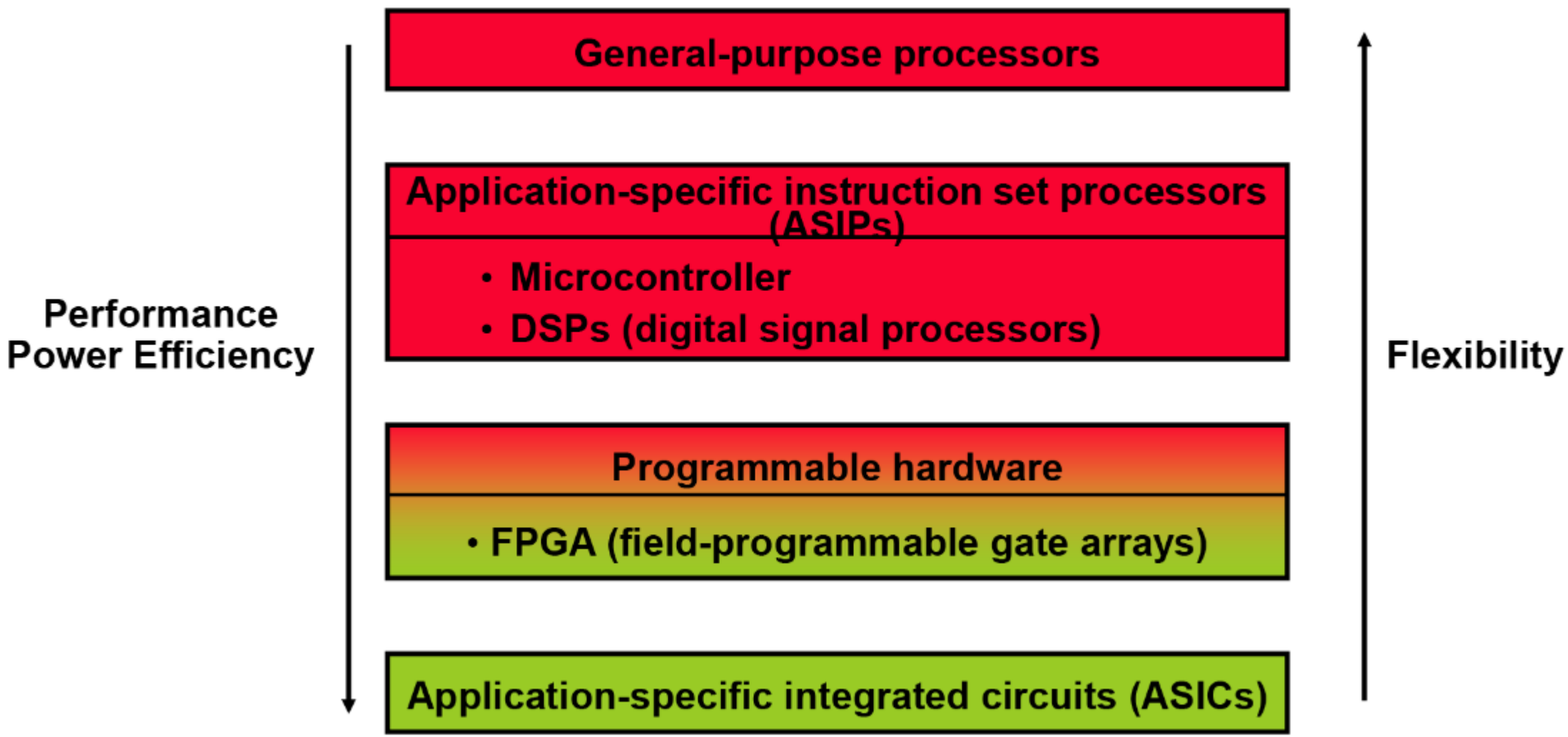
Software vs. Hardware Trade-offs



Distinct Features of Hardware and Software Design

	Hardware	Software
Design Paradigm	Decomposition in space	Decomposition in time
Resource	Area (#gates, #Slices)	Time (#Cycles)
Flexibility	Must be designed in	Implicit
Parallelism	Implicit	Must be designed in
Modeling	Model ≠ Implementation	Model ≈ Implementation
Reuse	Uncommon	Common

Codesign


General-purpose processors
Application-specific instruction set processors (ASIPs)
• Microcontroller
• DSPs (digital signal processors)
Programmable hardware
• FPGA (field-programmable gate arrays)
Application-specific integrated circuits (ASICs)
Performance
Power Efficiency
Flexibility

Codesign

- The First Generation:

  Vulcan approach and The Cosyma design system approach.

  partitioning a given functional specification.

  both assumed that the implementation was single-threaded and that the CPU and ASIC worked mutually exclusively into hardware and software.

- The second generation:

  HW/SW partitioning was elaborated on more and extended considerably for more complex types of architectures, including more than one CPU, but also the assumption of just single-threaded program execution was extended to multiprogramming and multiprocessing. Finally, also cosimulation.

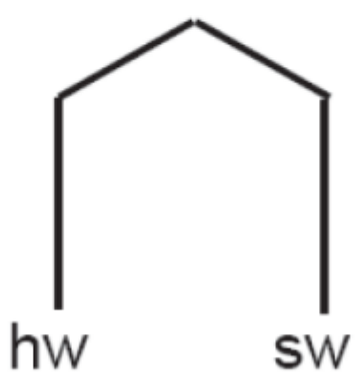
- The third generation:

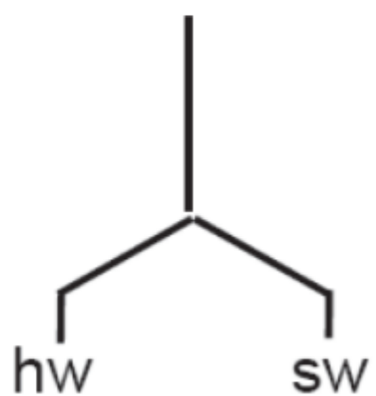
  hundle multiprogramming and multiprocessing regarding: Heterogeneous SoC, Hardware and software complexity, and subsystems Integration.

Codesign

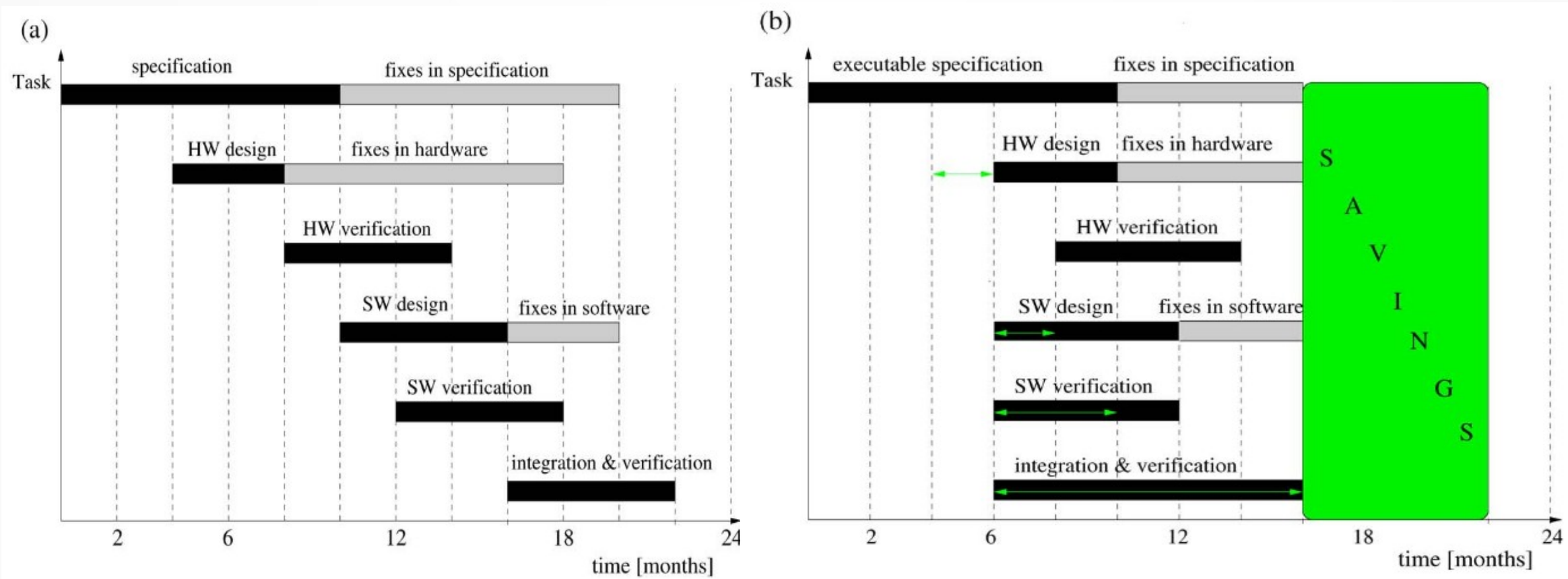
classic design

co-design

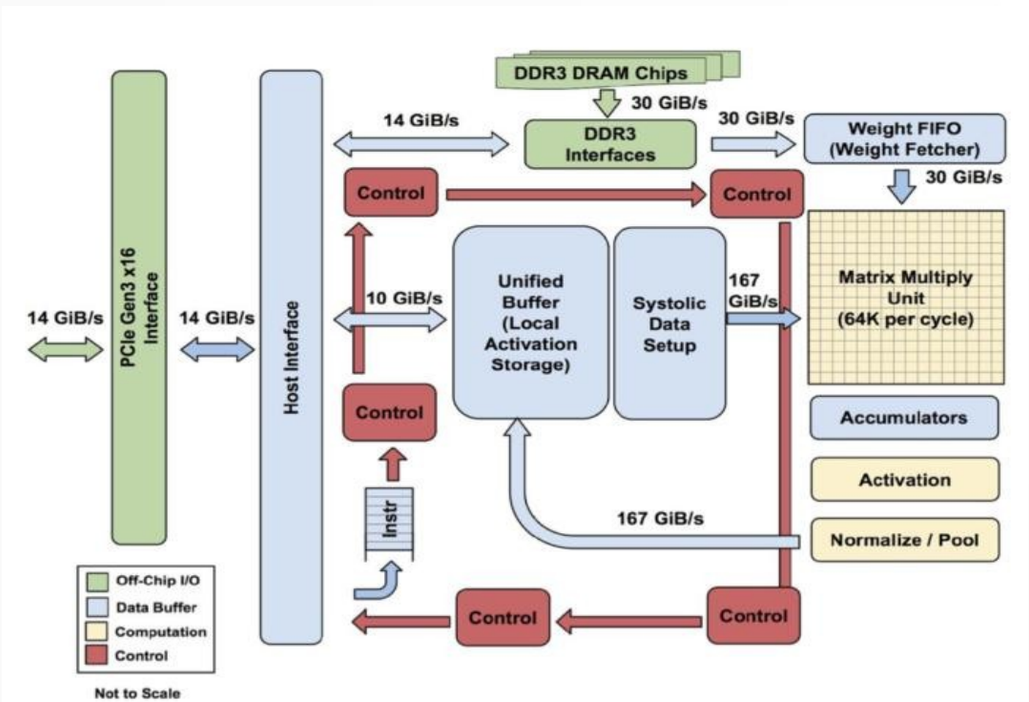


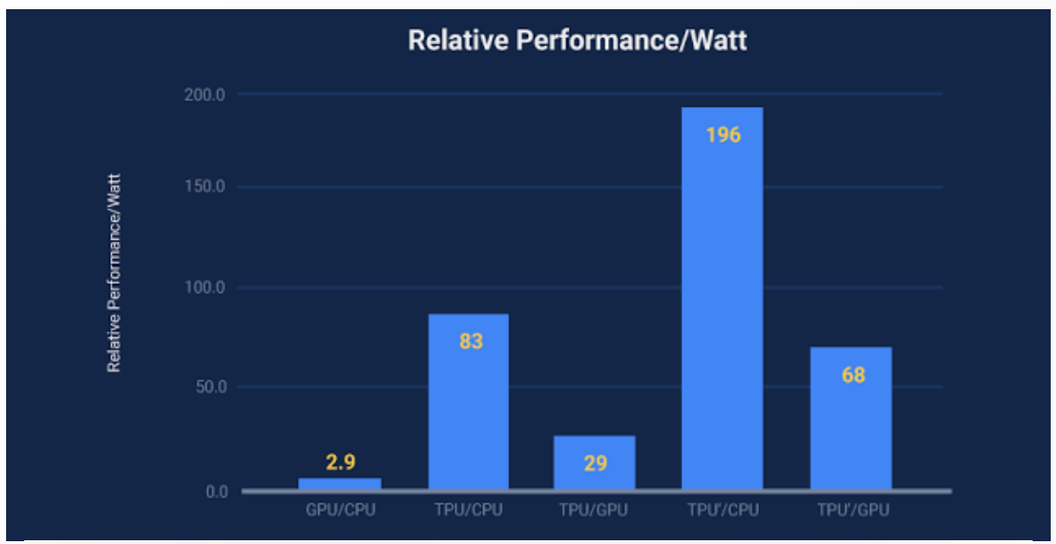


Codesign

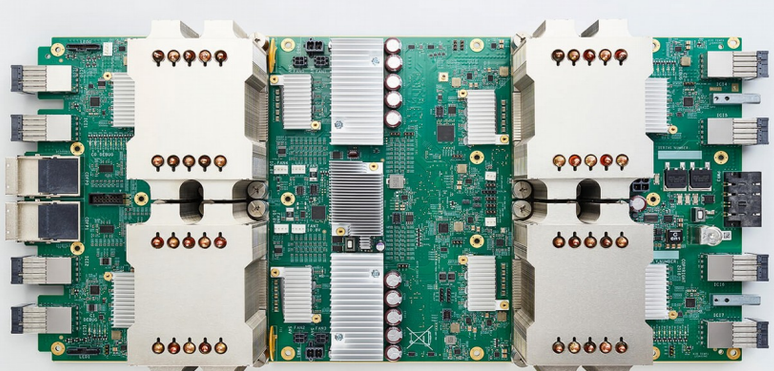

(a)
Task
specification
fixes in specification
HW design
fixes in hardware
HW verification
SW design
fixes in software
SW verification
integration & verification
2
6
12
18
24
time [months]
(b)
Task
executable specification
fixes in specification
HW design
fixes in hardware
HW verification
SW design
fixes in software
SW verification
integration & verification
SAVINGS
2
6
12
18
24
time [months]

Google TPU

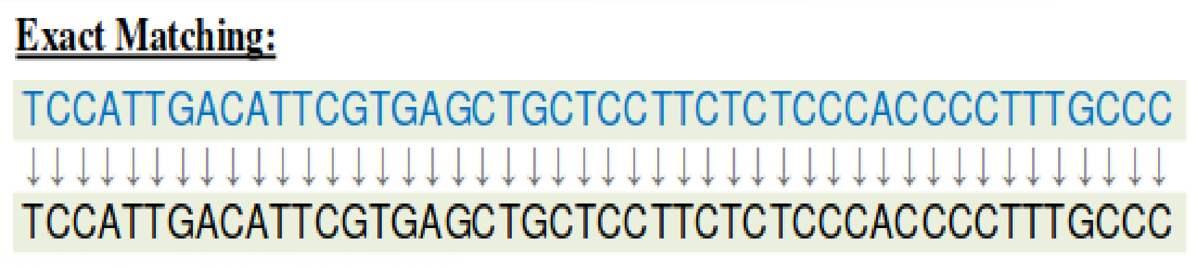


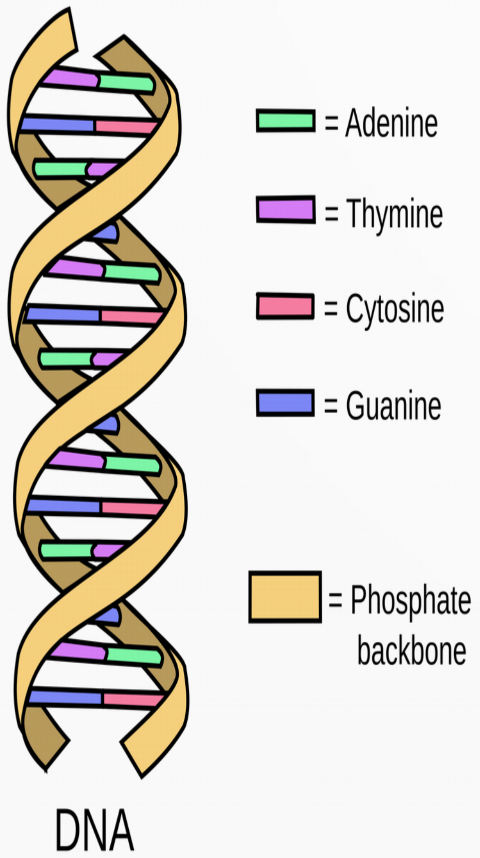


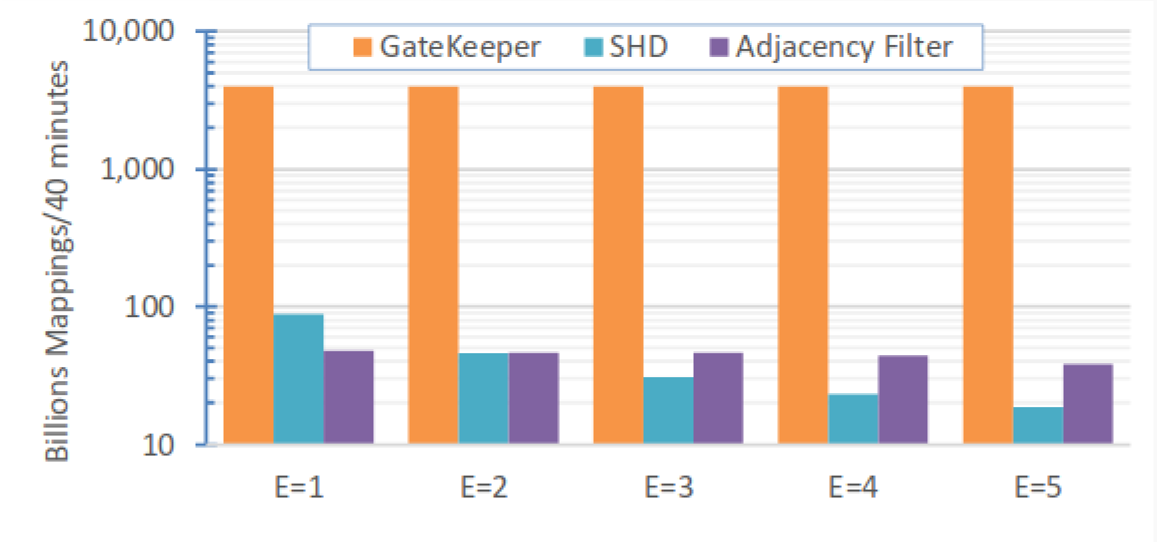
- The TPU is not a general-purpose device like an Intel CPU or Nvidia GPU. It is an application-specific integrated circuit (ASIC) designed for machine learning, a specialized subfield of artificial intelligence.



GateKeeper

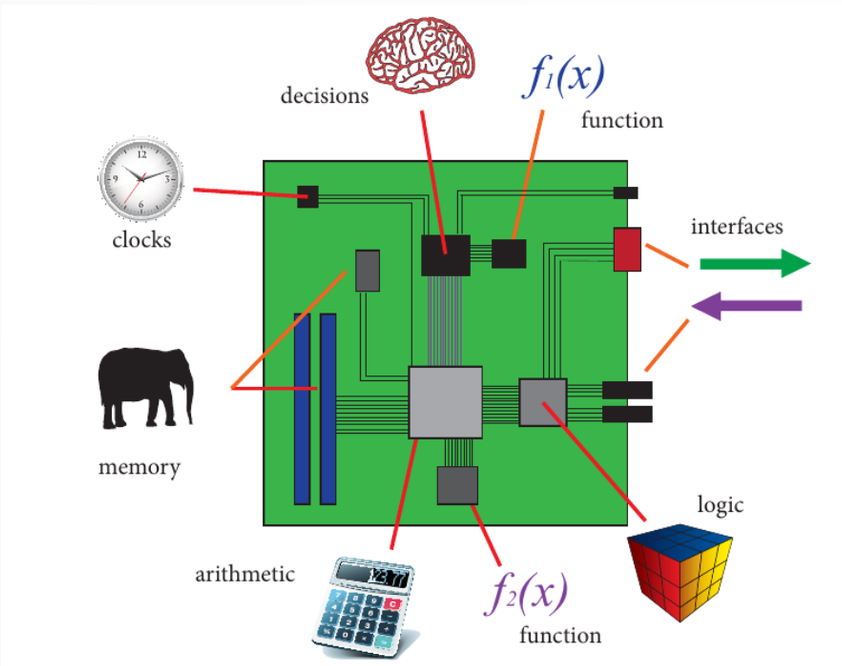


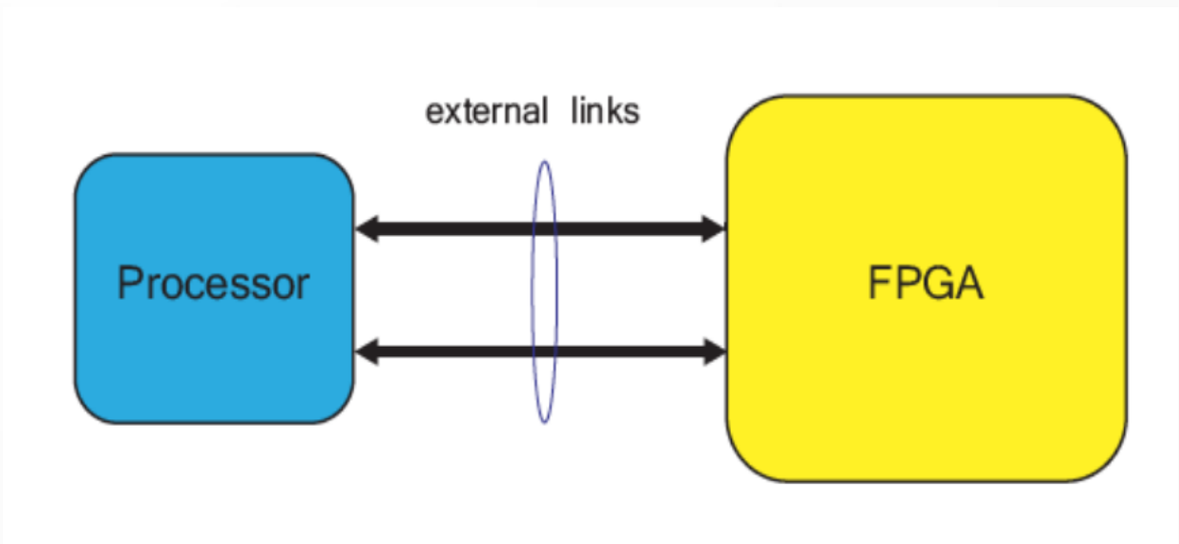




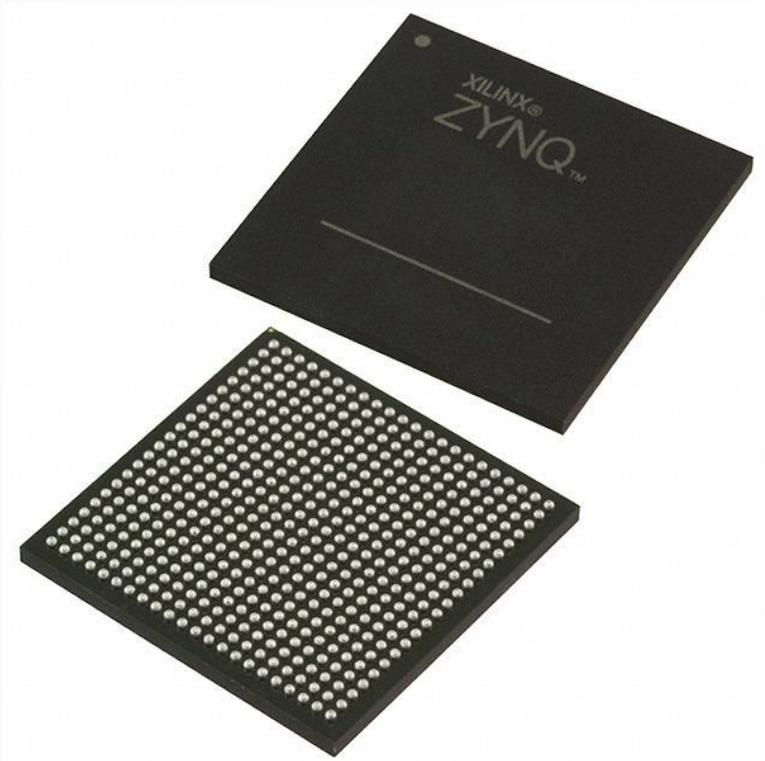
- A hardware accelerator that functions as a pre-alignment step that quickly filters out most incorrect candidate locations. GateKeeper is the first design to ac-celerate pre-alignment using Field-Programmable Gate Arrays (FPGAs), which can perform pre-alignment much faster than software. GateKeeper can be integrated with any mapper that per-forms sequence alignment for verification.

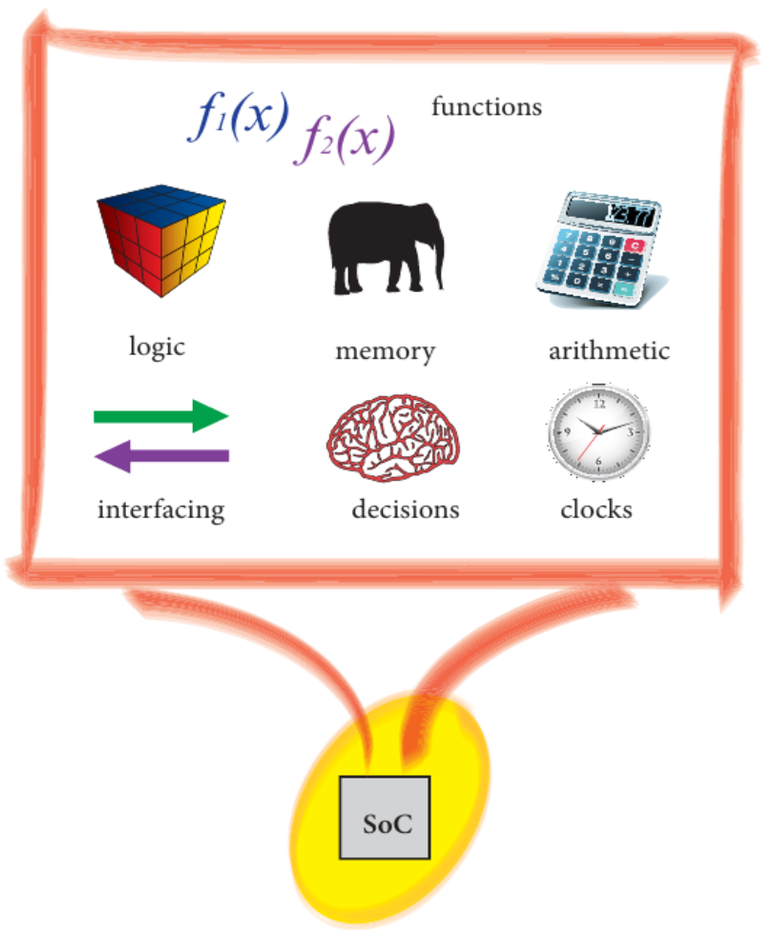
System on board



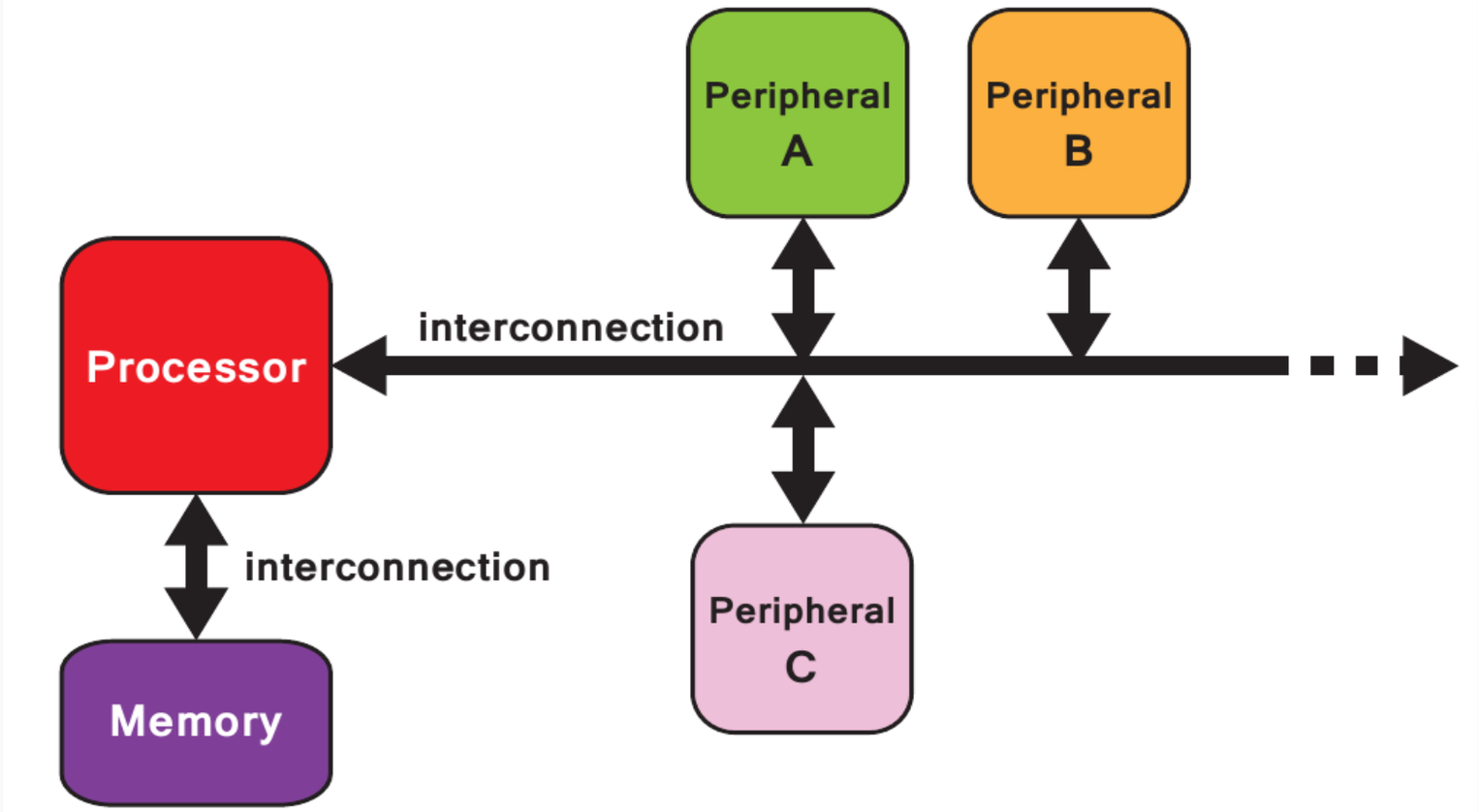


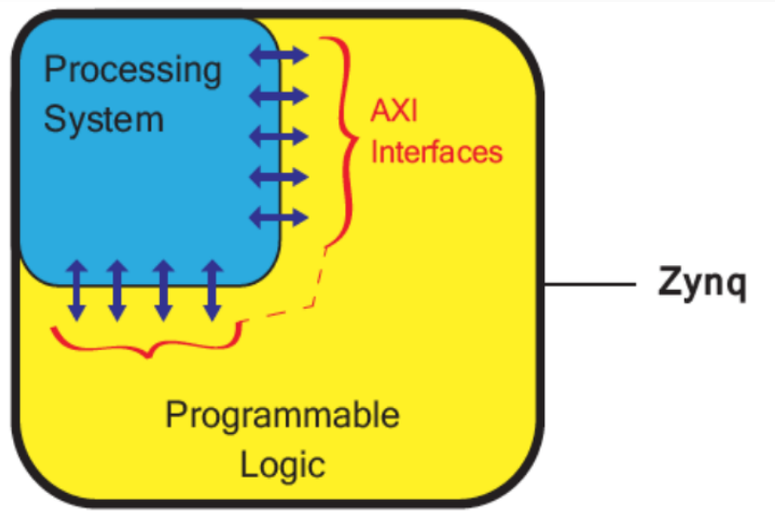
System on chip

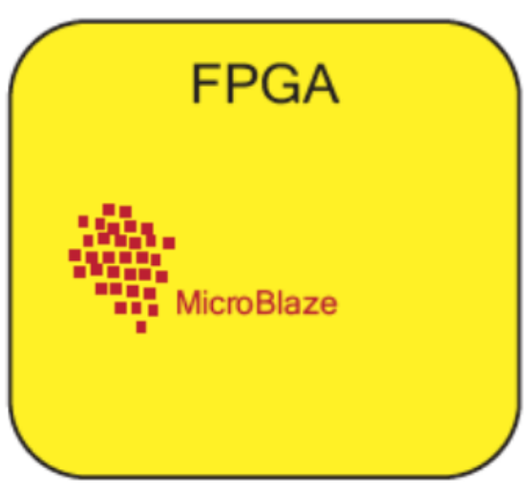




System on chip



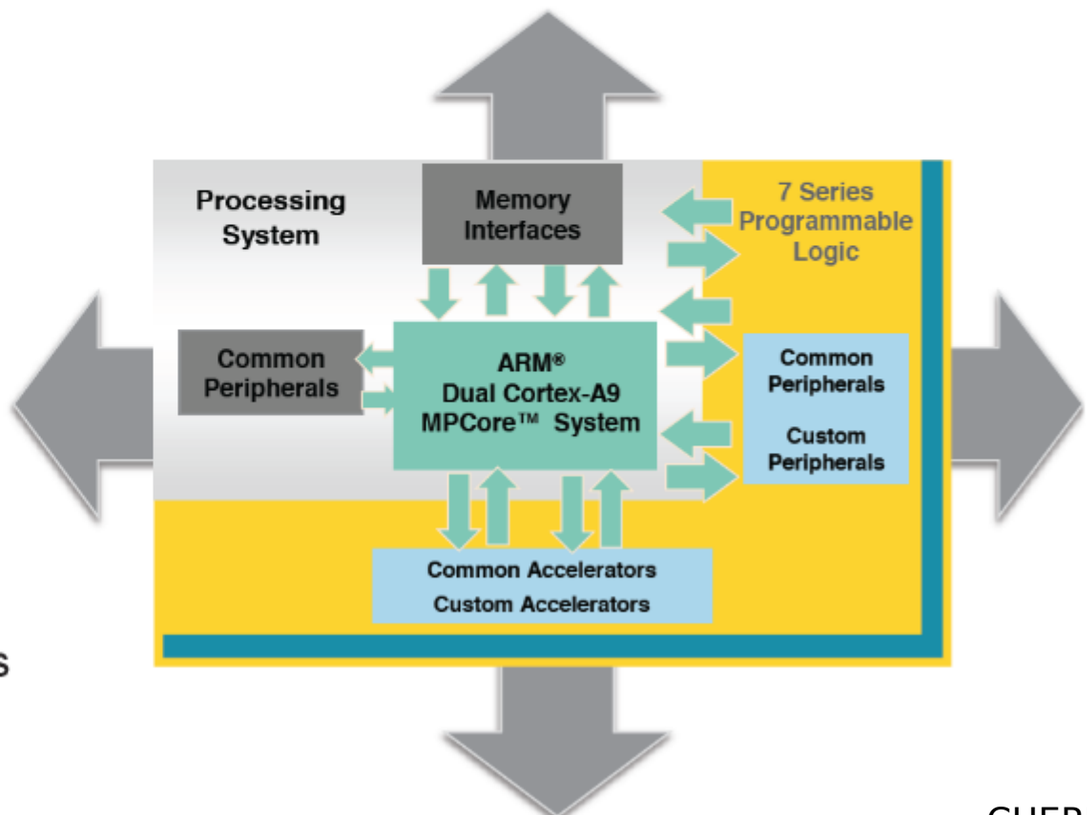




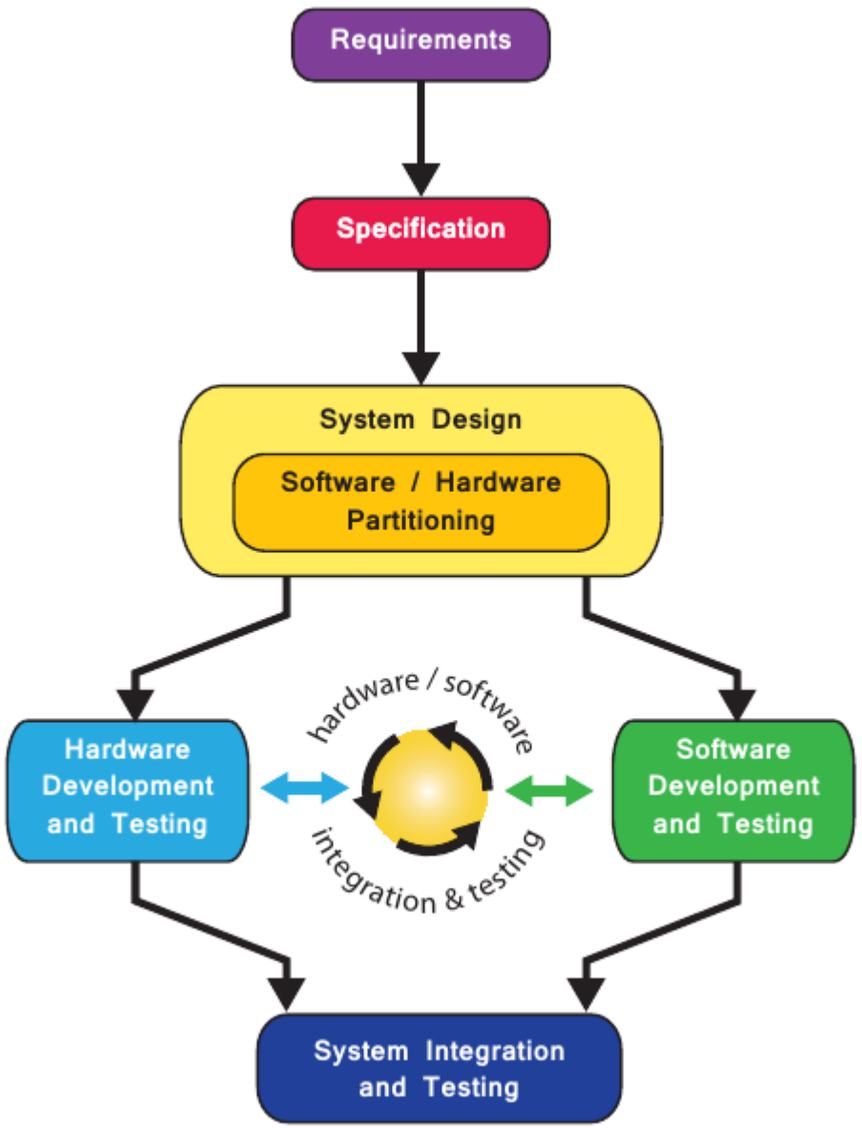
Zynq

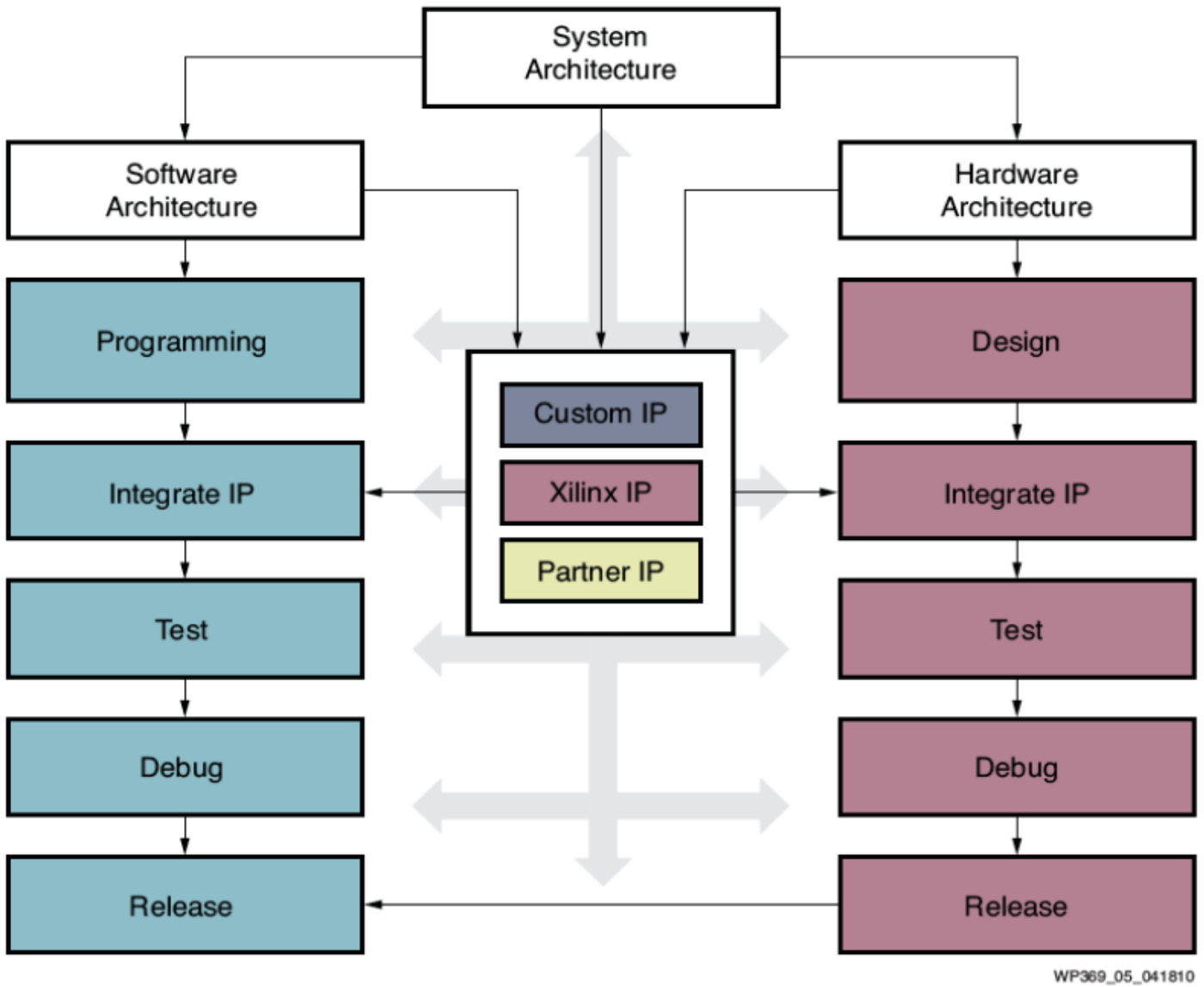
- **Complete ARM®-based Processing System**
  - Dual ARM Cortex™-A9 MPCore™, processor centric
  - Integrated memory controllers & peripherals
  - Fully autonomous to the Programmable Logic
- **Tightly Integrated Programmable Logic**
  - Used to extend Processing System
  - High performance ARM AXI interfaces
  - Scalable density and performance
- **Flexible Array of I/O**
  - Wide range of external multi-standard I/O
  - High performance integrated serial transceivers
  - Analog-to-Digital Converter inputs

ZYNQ™



Basic Design Flow for Zynq SoC





Alternative socs

because they hav

Xilinx Zynq

Zynq-7000 All Programmable SoCs with Cortex-A9 MPCore

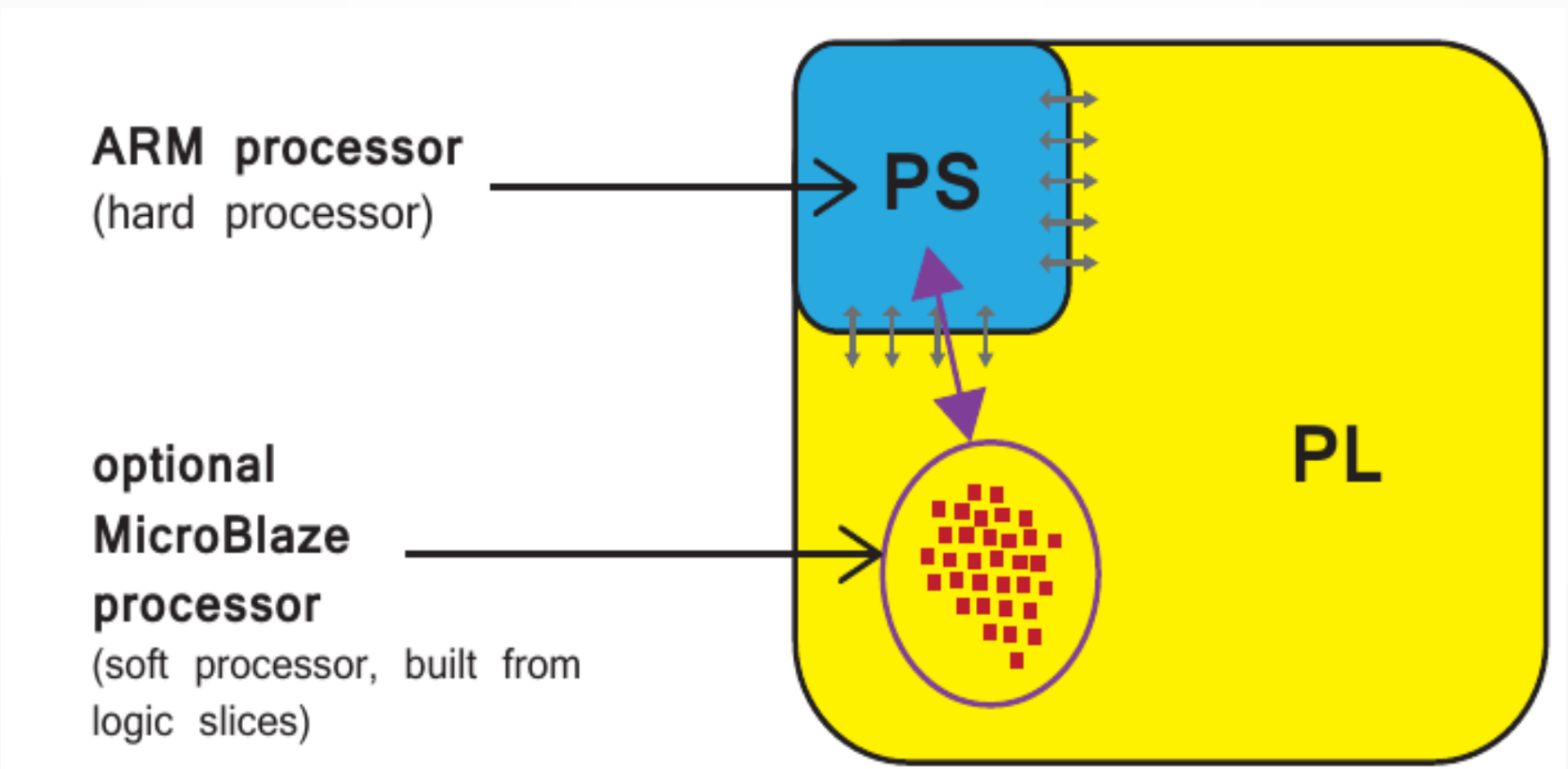
Altera Arria V & Cyclone V

Hard processor system (HPS) with Cortex-A9 MPCore

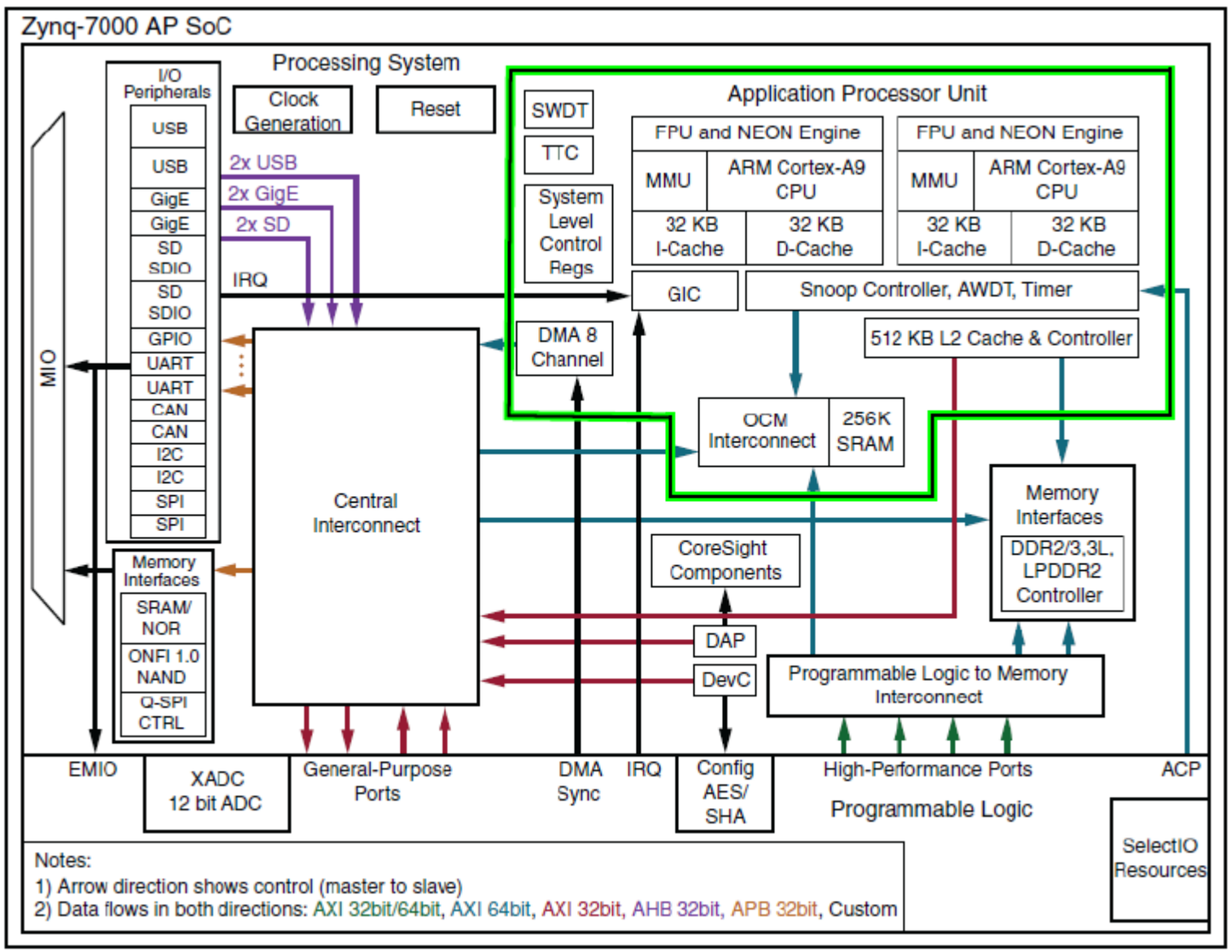
Microsemi Smartfusion2

Cortex M3

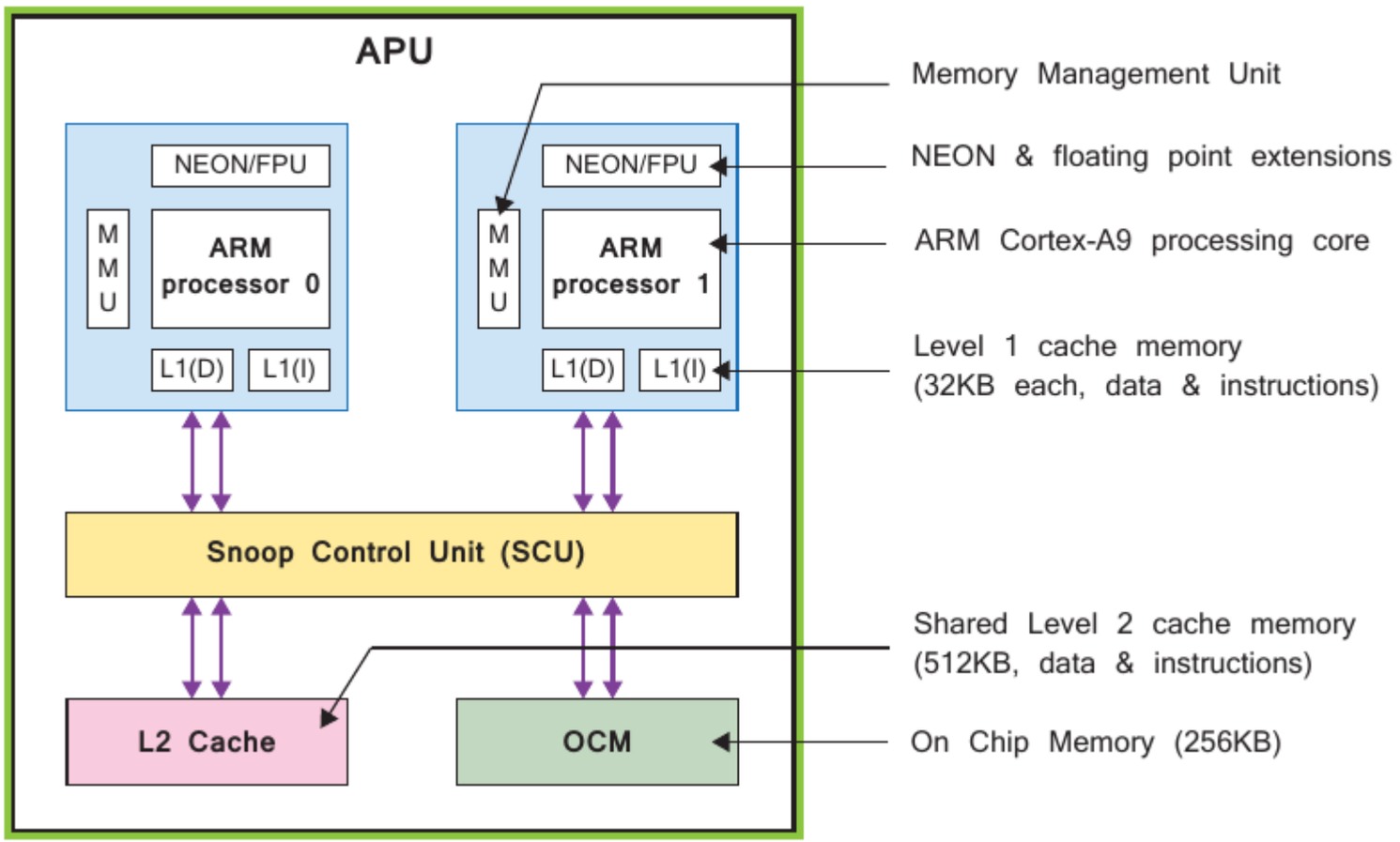
Zynq


ARM processor
(hard processor)
optional
MicroBlaze
processor
(soft processor, built from
logic slices)
PS
PL

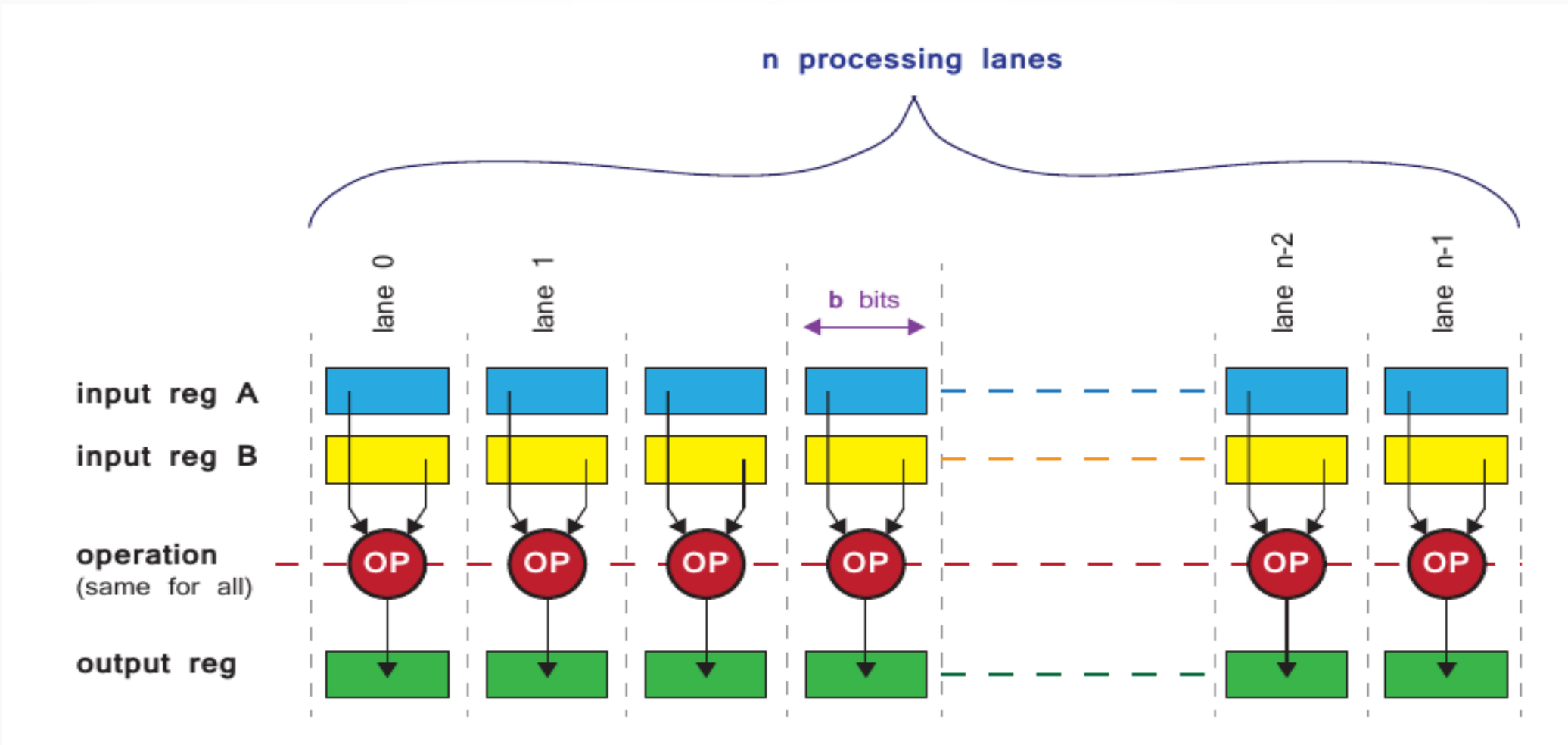
Zynq PS


Zynq-7000 AP SoC
Processing System
I/O Peripherals
USB
USB
GigE
GigE
SD SDIO
SD SDIO
GPIO
UART
UART
CAN
CAN
I2C
I2C
SPI
SPI
MIO
Clock Generation
Reset
2x USB
2x GigE
2x SD
IRQ
Application Processor Unit
SWDT
TTC
System Level Control Regs
FPU and NEON Engine
MMU
ARM Cortex-A9 CPU
32 KB I-Cache
32 KB D-Cache
FPU and NEON Engine
MMU
ARM Cortex-A9 CPU
32 KB I-Cache
32 KB D-Cache
GIC
Snoop Controller, AWDT, Timer
512 KB L2 Cache & Controller
DMA 8 Channel
OCM Interconnect
256K SRAM
Central Interconnect
Memory Interfaces
DDR2/3,3L, LPDDR2 Controller
CoreSight Components
DAP
DevC
Programmable Logic to Memory Interconnect
Memory Interfaces
SRAM/ NOR
ONFI 1.0 NAND
Q-SPI CTRL
EMIO
XADC 12 bit ADC
General-Purpose Ports
DMA Sync
IRQ
Config AES/ SHA
High-Performance Ports
ACP
Programmable Logic
SelectIO Resources
Notes:
1) Arrow direction shows control (master to slave)
2) Data flows in both directions: AXI 32bit/64bit, AXI 64bit, AXI 32bit, AHB 32bit, APB 32bit, Custom
DS190_01_030713
© Xilinx

Application processing unit

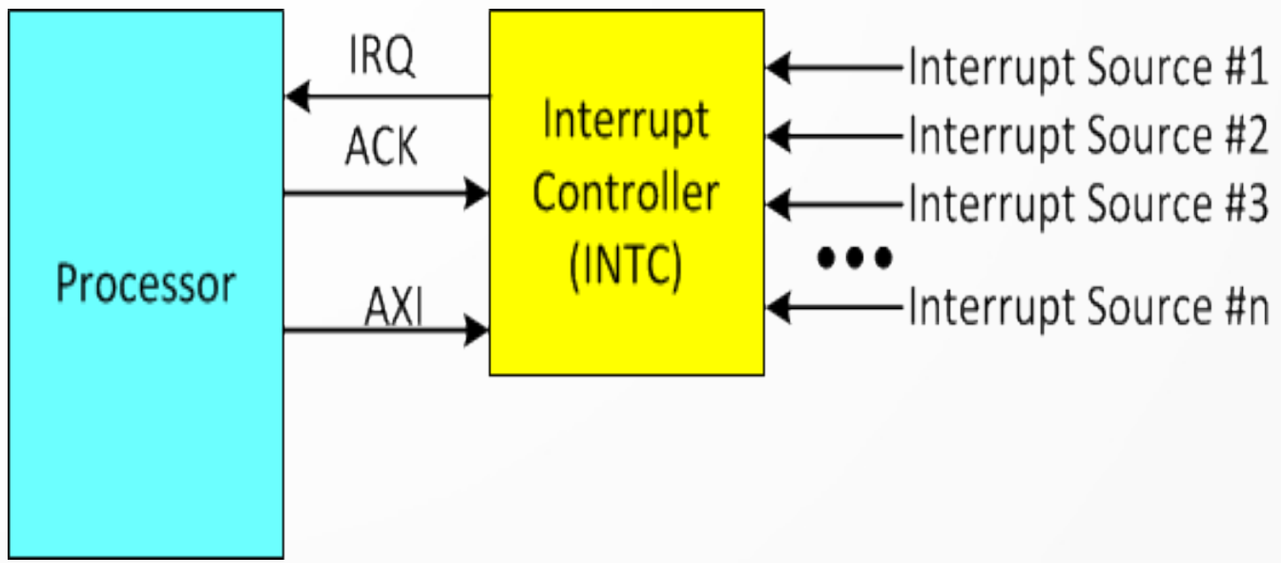


SIMD (Single Instruction Multiple Data) Processing in the NEONMedia Processing Engine (MPE)



Zynq PS

I/O Interface	Description
SPI (x2)	Serial Peripheral Interface [10] *De facto standard for serial communications based on a 4-pin interface. Can be used either in master or slave mode.*
I2C (x2)	I^2C bus [14] *Compliant with the I2C bus specification, version 2. Supports master and slave modes.*
CAN (x2)	Controller Area Network *Bus interface controller compliant with ISO 118980-1, CAN 2.0A and CAN 2.0B standards.*
UART (x2)	Universal Asynchronous Receiver Transmitter *Low rate data modem interface for serial communication. Often used for Terminal connections to a host PC.*
GPIO	General Purpose Input/Output *There are 4 banks GPIO, each of 32 bits.*
SD (x2)	*For interfacing with SD card memory.*
USB (x2)	Universal Serial Bus *Compliant with USB 2.0, and can be used as a host, device, or flexibly ("on-the-go" or OTG mode, meaning that it can switch between host and device modes).*
GigE (x2)	Ethernet *Ethernet MAC peripheral, supporting 10Mbps, 100Mbps and 1Gbps modes.*



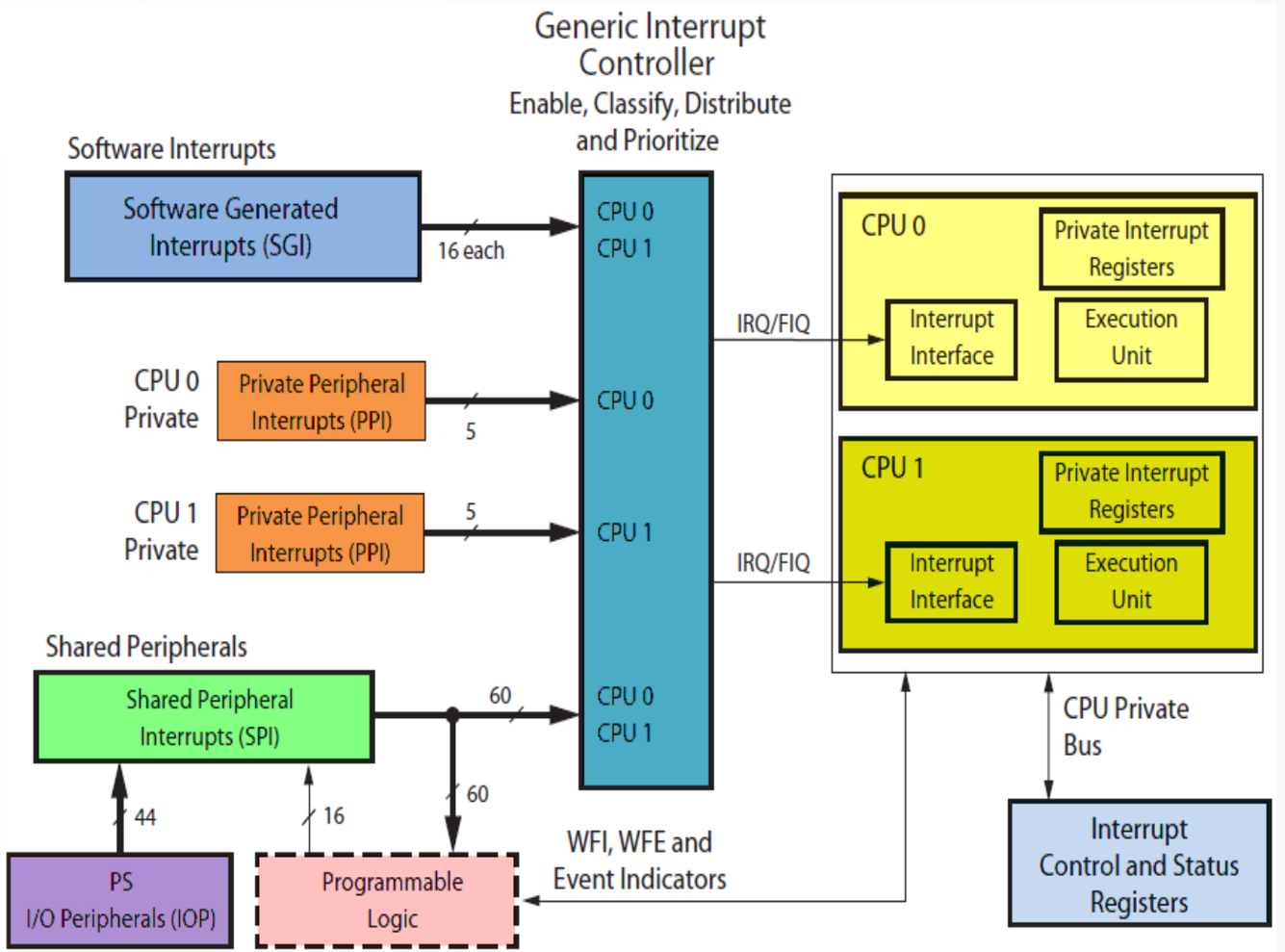
The GIC has four primary responsibilities over interrupt sources

Enable, Classify, Prioritize, and Distribute

Zynq PS

Interrupt controllers are hardware devices that:

- Collect multiple interrupts from external sources
- Prioritize simultaneously occurring interrupts so that the uP handles the most important interrupt first
- Manages new interrupts that the uP is currently executing as an interrupt handler
- Present prioritized interrupts one-at-a-time to the microprocessor
- Provide information as to which interrupt occurred



Zynq ps

Triple time counter two main uses are:

- Digital signal generation(PWM).
- Periodic interrupts.

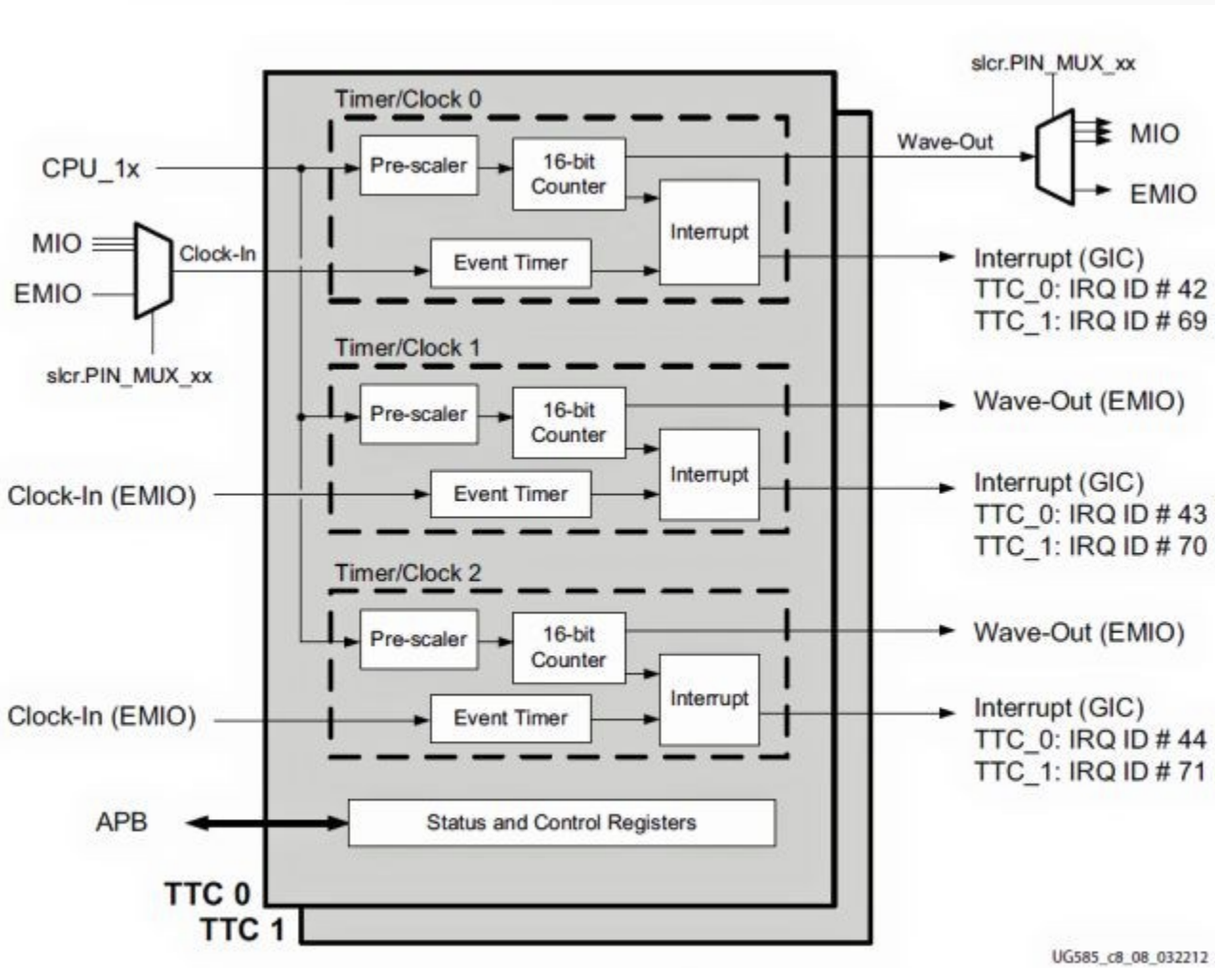
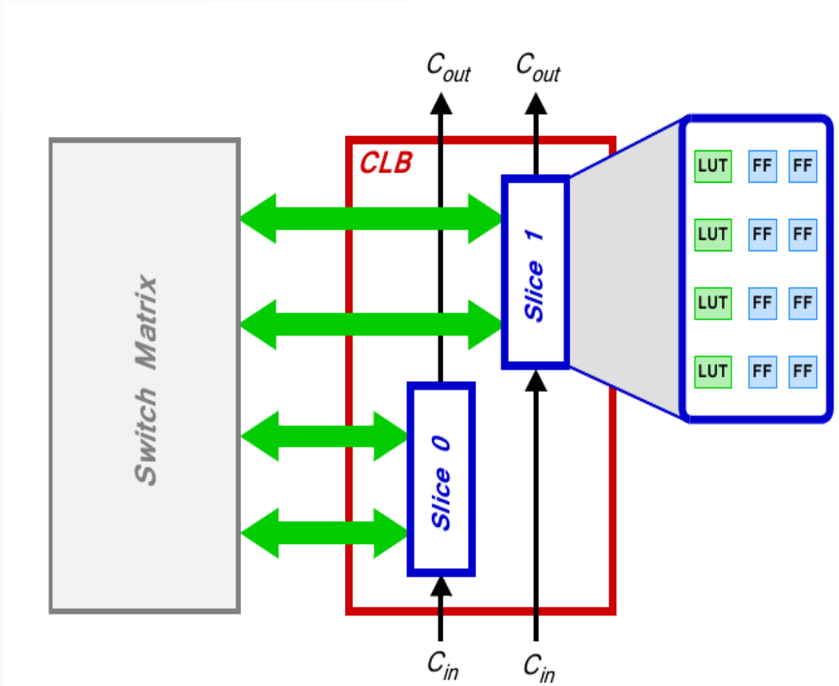
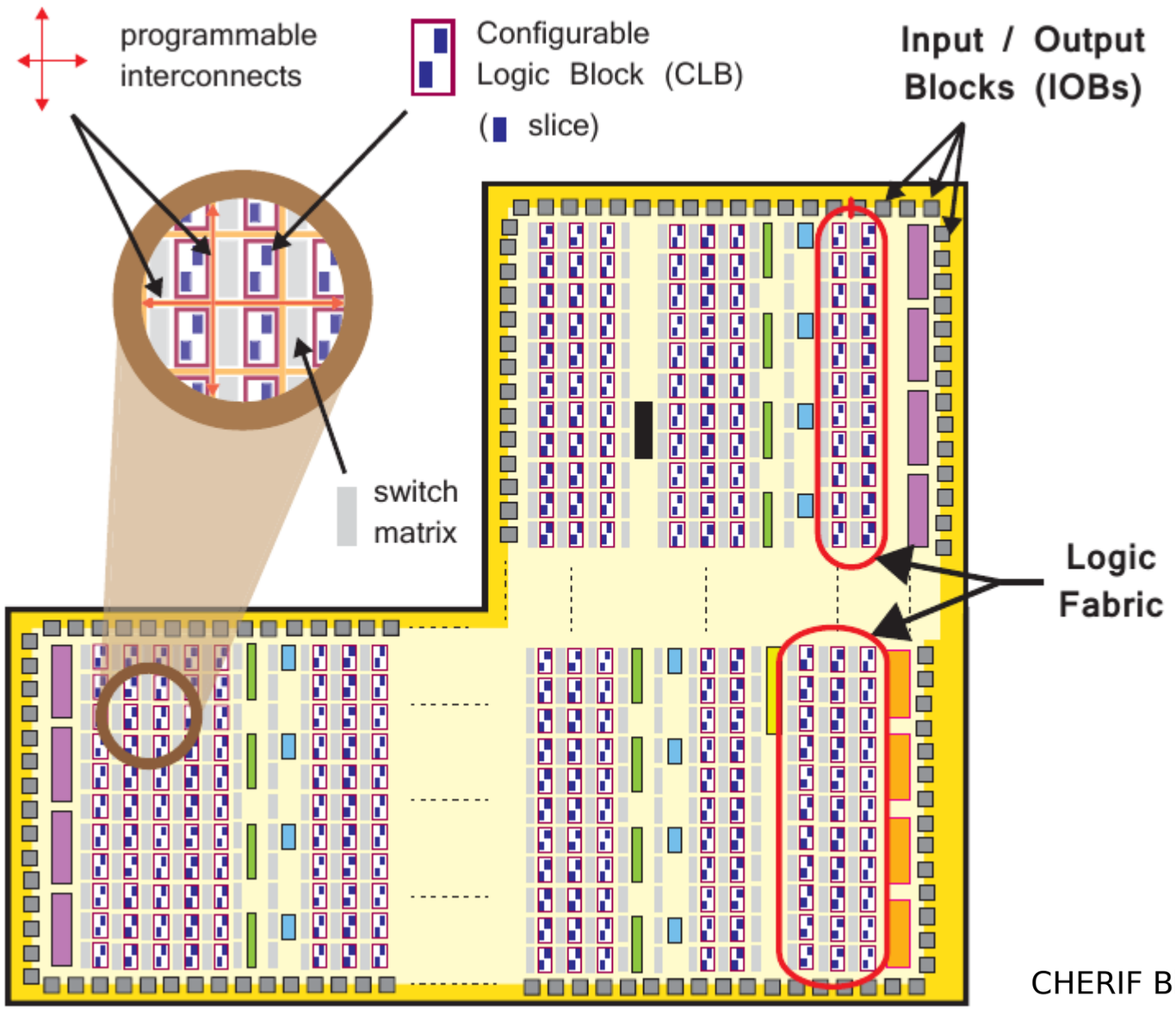


Figure 8-3: **Triple Counter Timer Block Diagram**

Zynq PL


C_{out}
C_{out}
CLB
Switch Matrix
Slice 1
Slice 0
LUT
FF
C_{in}
C_{in}


programmable interconnects
Configurable Logic Block (CLB)
(slice)
Input / Output Blocks (IOBs)
switch matrix
Logic Fabric

Zynq PL

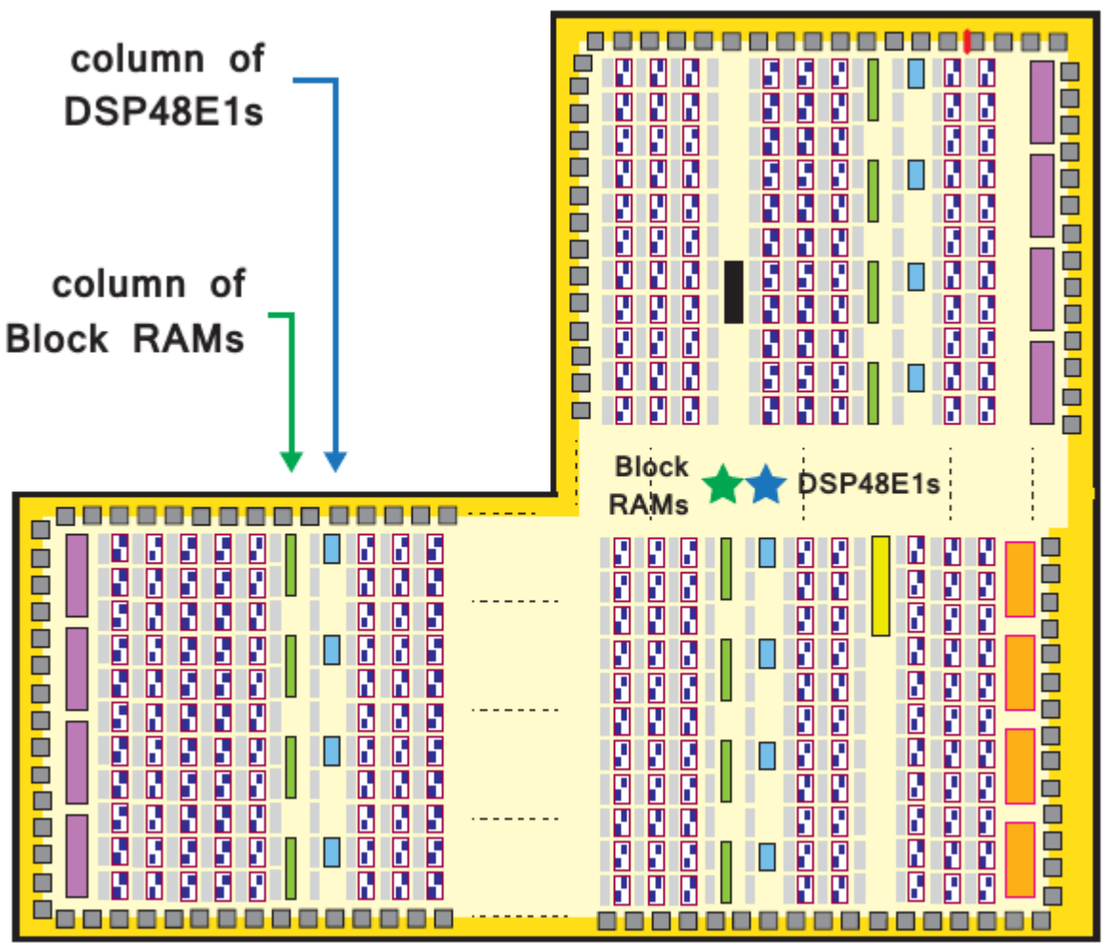
Block RAM serves as a relatively large memory structure used whenever you need to store a bunch of data on a chip. Here are a few examples:

- A part of a FIFO between two clock domains.

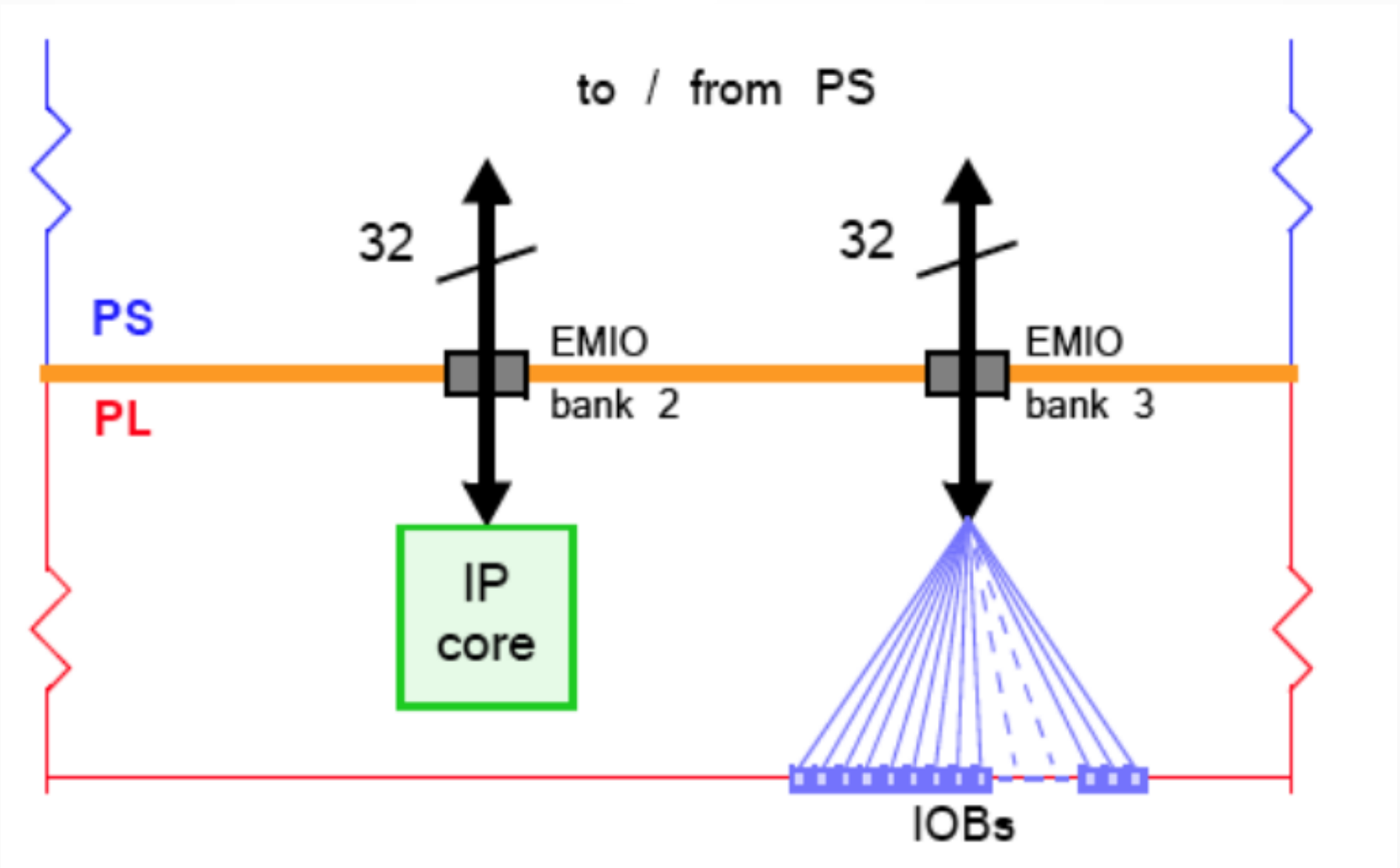
- A video frame or data packet buffer in a communications system.

- Large LUT.

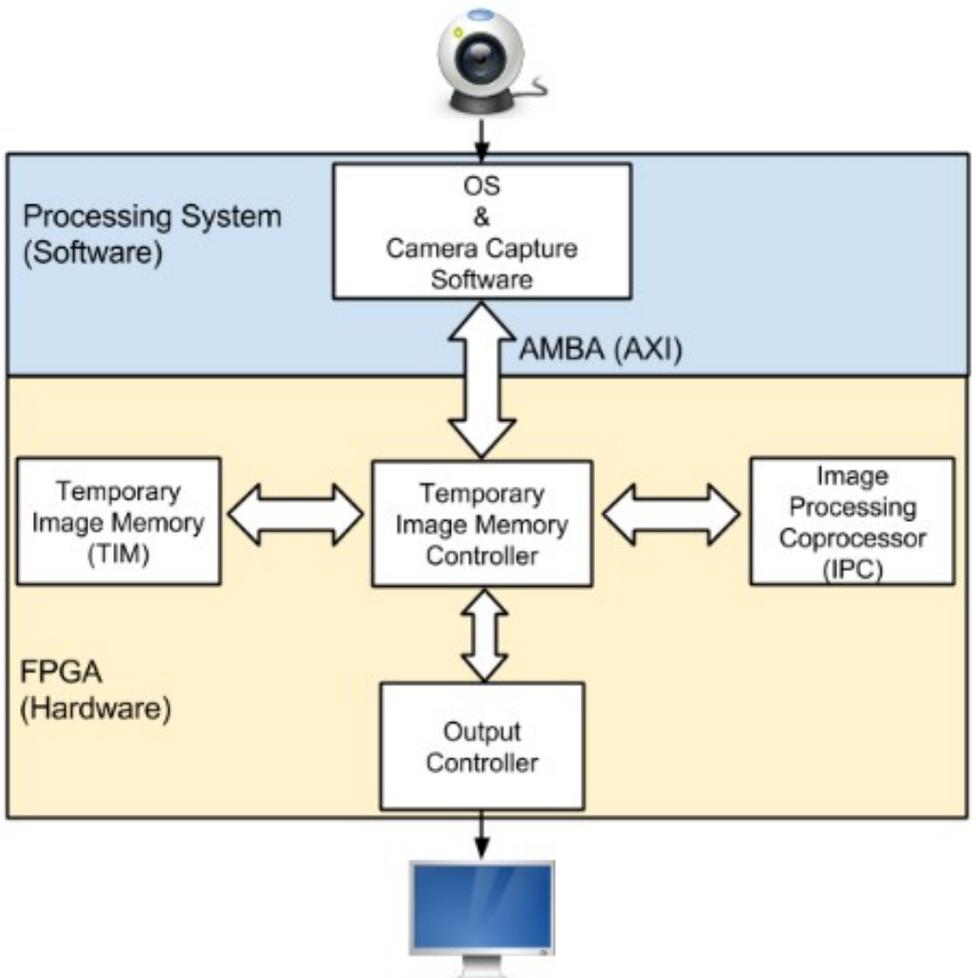
DSP48E1s slice can be used to perform different kinds of arithmetic operations.You also can use the slice to perform different kinds of logic operations. You can cascade multiple DSP48E slices to implement more complex functions without using any additional FPGA fabric resources.

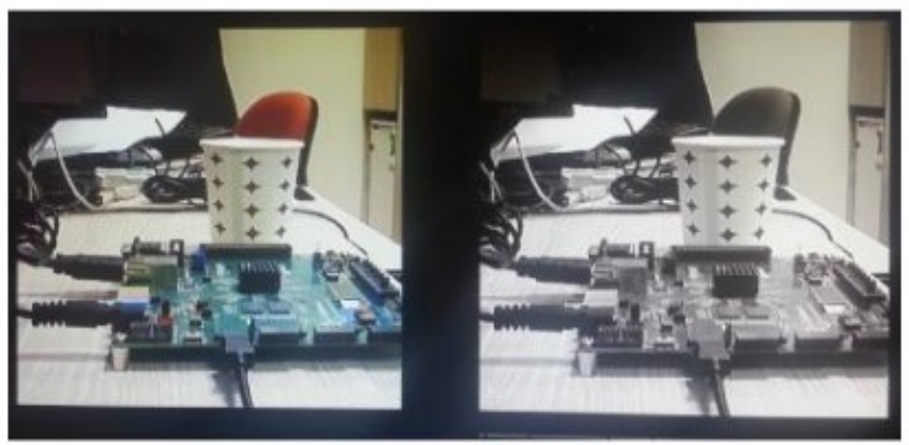


Zynq PL-PS EMIO

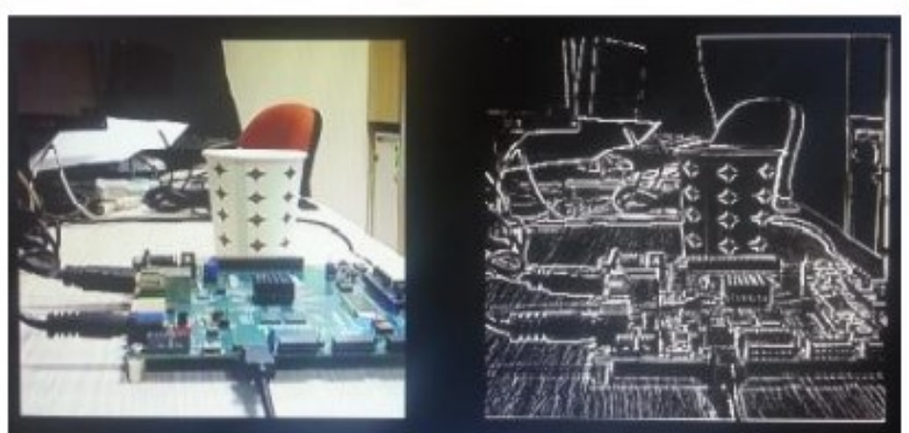


Real-Time System Implementation for Image Processing with Hardware/Software Co-design on the Xilinx Zynq Platform





Grayscale



Edge Detection

Thank you :)